Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OUTPUT A**
2. **– INPUT A**
3. **+ INPUT A**
4. **GND**
5. **+ INPUT B**
6. **– INPUT B**
7. **OUTPUT B**
8. **VCC+**

**.044”**

**1 2 3**

**4**

**7 6 5**

**8**

**MASK**

**REF**

**.054”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 358E**

**APPROVED BY: DK DIE SIZE .044” X .054” DATE: 9/22/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: LM158**

**DG 10.1.2**

#### Rev B, 7/1